

# PATENT ABSTRACTS OF JAPAN

(11)Publication number : 07-134223

(43)Date of publication of application : 23.05.1995

(51)Int.Cl.

G02B 6/42

(21)Application number : 05-279967

(71)Applicant : FUJITSU LTD

(22)Date of filing : 10.11.1993

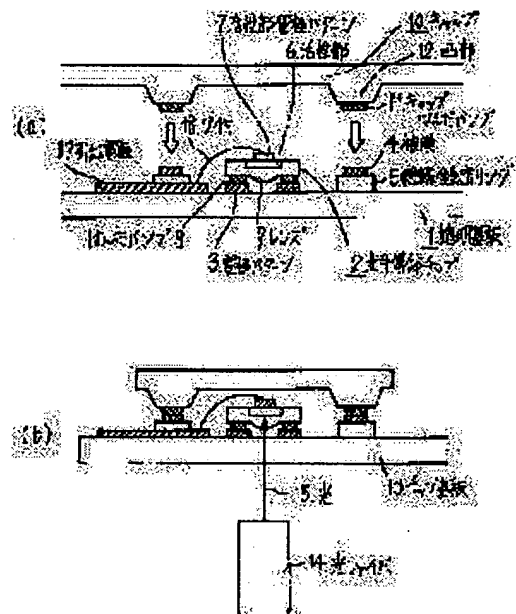
(72)Inventor : TABUCHI HARUHIKO

## (54) PRODUCTION OF OPTICAL SEMICONDUCTOR DEVICE

### (57)Abstract:

**PURPOSE:** To shorten the processing stage by integrally and simultaneously executing hermetic sealing of many pieces of optical semiconductor chips in the process for production of a light emitting device and a light receiving device for optical communication formed by using the optical semiconductor chips and more particularly hermetic sealing of the optical semiconductor chips into the optical semiconductor device.

**CONSTITUTION:** A gap 10 having projecting parts 12 two-dimensionally formed in correspondence to insulating rings 5 on the rear surface is aligned and soldered to a transparent substrate 1 formed by two-dimensionally arranging the plural optical semiconductor chips 2 on the transparent substrate 1 and is soldered to integrally and hermetically seal the plural optical semiconductor chips 2. Further, an optical fiber device having a light reflecting means for bending the light 15 emitted from an optical fiber 14 in the direction perpendicular to the optical axis of the optical fiber 14 is adhered to the transparent substrate 1.



## LEGAL STATUS

[Date of request for examination] 14.01.2000

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number] 3277646

[Date of registration] 15.02.2002

[Number of appeal against examiner's decision of rejection]

BEST AVAILABLE COPY

[Date of requesting appeal against examiner's  
decision of rejection]

[Date of extinction of right]

Copyright (C); 1998,2003 Japan Patent Office

JPO and NCIP are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. \*\*\*\* shows the word which can not be translated.
3. In the drawings, any words are not translated.

## DETAILED DESCRIPTION

---

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to the hermetic seal into the manufacture approach of the luminescence equipment for optical communication which uses an optical semiconductor chip, and light-receiving equipment, especially the optical semiconductor device of an optical semiconductor chip.

[0002]

[Description of the Prior Art] Drawing 7 is the explanatory view of the conventional example. drawing -- setting -- 2 -- an optical semiconductor chip and 3 -- an electrode pattern and 6 -- the activity section and 7 -- an activity section electrode pattern and 8 -- a solder bump and 9 -- a lens and 10 -- a cap and 14 -- an optical fiber and 15 -- for a wire and 25, as for lead wire and 27, a block and 26 are [ light and 17 / a drawer electrode and 18 / an insulating material and 28 ] apertures.

[0003] Conventionally, as shown in drawing 7 , after carrying out bonding of the optical semiconductor chip 2 to the block 25 to which lead wire 26 and electrode pattern 3 grade were attached, the transparent cap 10 with aperture 28 which penetrates the light 15 from an optical fiber 14 was welded to the block 25, and the hermetic seal was performed.

[0004]

[Problem(s) to be Solved by the Invention] However, it is necessary to stick the chip-like aperture 28 on cap 10, and the process of shaping of an aperture 28, metallizing, and lamination is needed by such approach in that case. Therefore, the one-piece \*\*\*\*\* sake took time and effort every optical semiconductor chip 2 in these processes, and there was a problem that productivity was bad and the yield also fell.

[0005] Moreover, in order to make enlarging reinforcement of an aperture 28, and the coefficient of thermal expansion of an aperture 28 in agreement with cap 10, expensive ingredients, such as sapphire, were used for the ingredient of an aperture 27, and it was expensive also on the cap 10 and ingredients, such as covar with bad workability, were used for it.

[0006] Therefore, the problem that the cost of ingredient components became large was produced. Furthermore, by the conventional approach, since both the bonding of the optical semiconductor chip 2 and every one hermetic seal of cap 10 were performed, the limitation was in mass-production nature.

[0007] This invention was offered in view of such a trouble, bundles up the hermetic seal of many optical semiconductor chips, performs it to coincidence, and aims at offering the manufacture approach of the optical semiconductor device which shortens a process.

[0008]

[Means for Solving the Problem] Drawing 1 is the principle explanatory view of this invention, and drawing 2 is the explanatory view of the 1st example of this invention. drawing -- setting -- 1 -- a transparence substrate and 2 -- an optical semiconductor chip and 3 -- an electrode pattern and 4 -- a coat and 5 -- an insulating airtight ring and 6 -- the activity section and 7 -- an activity section electrode pattern and 8 -- a solder bump and 9 -- a lens and 10 -- a cap and 11 -- a cap solder bump and 12 -- for an optical fiber and 15, as for optical fiber equipment and 17, light and 16 are [ heights and 13 / a chip substrate and 14 / a drawer electrode and 18 ] wires.

[0009] In order to solve the above-mentioned trouble, after carrying a majority of two or more optical semiconductor chips 2 in the one wafer-like transparence substrate 1 two-dimensional by the approach of this invention, soldering the cap which consists of one substrate too by the approach of this invention and performing the package coincidence hermetic seal of an optical semiconductor chip, a cap and a transparence substrate are cut and an optical semiconductor device is obtained.

[0010] Namely, two or more electrode patterns 3 which have solder wettability on the transparence substrate 1 as the purpose of this invention is shown in drawing 1 (a), The process which forms the insulating airtight ring 5 on which the coat 4 which has solder wettability in the periphery of this electrode pattern 3 was put, The process which positions and solders this solder bump 8 of this optical semiconductor chip 2 that has two or more solder bumps 8 and the convex lens 9 at the rear face to this electrode pattern 2, As it is indicated in drawing 1 (b) as the process which solders this cap solder bump 11 of cap 10 that has the cap solder bump 11 to an inferior surface of tongue, and carries out the hermetic seal of this optical semiconductor chip 2 to this insulating airtight ring 5 By including the process which separates this cap 10 this each optical semiconductor chip 2 of every on the outside of this insulating airtight ring 5, then separates this transparence substrate 1 to the chip substrate 13 containing this each optical semiconductor chip 2 Moreover, as shown in drawing 2 (a), as shown in said transparence substrate 1 which arranged and was soldered on said transparence substrate 1 two-dimensional at drawing 1 (a), said two or more optical semiconductor chips 2 By carrying out alignment of the cap 10 which has said cap solder bump 11 formed in the inferior surface of tongue two-dimensional corresponding to said insulating ring 5, soldering it, and carrying out the hermetic seal of these two or more optical semiconductor chips 2 collectively Furthermore, as shown in the example of drawing 3 - drawing 6 , it is attained by pasting up the optical fiber equipment 16 which has a light reflex means to bend the optical axis of this optical fiber 14 on said transparence substrate 1 so that incidence of the light 15 by which outgoing radiation was carried out from the optical fiber 14 may be carried out to the lens 9 of said optical semiconductor chip 2.

[0011]

[Function] Since according to the means of this invention the transparence substrate with which many optical semiconductor chips were arranged two-dimensional, and much caps can use the cap arranged by two dimensions and can carry out a package hermetic seal now per wafer, productive efficiency goes up compared with the former, and the yield also improves.

[0012] Moreover, since batch processing also of metallizing processing of an aperture ingredient, bonding, and the wiring can be carried out now per wafer, it is suitable for

mass production method. And since the surface mount gestalt is taken, it is effective in it becoming easy to automate bonding using the mounting equipment for mounting components to up to the conventional printed circuit board. As a result, low cost-ization is realizable.

[0013]

[Example] Drawing 1 is the explanatory view of some examples of this invention, and shows the principle explanatory view of this invention, drawing 2 - drawing 6 except for the perspective view of drawing 2 in a type section Fig.

[0014] In drawing 1 an optical semiconductor chip and 3 for a transparence substrate and 2 An electrode pattern, In 4, a coat and 5 the activity section and 7 for an insulating airtight ring and 6 An activity section electrode pattern, In 8, a solder bump and 9 a cap, and 11 for a lens and 10 A cap solder bump, For a chip substrate and 14, an optical fiber and 15 are [ 12 / heights and 13 ] light, and 16 and 16a. Optical fiber equipment, 17 -- a drawer electrode and 18 -- for a photodiode array and 21, as for optical waveguide and 23, a glass substrate and 22 are [ a wire and 19 / an optical fiber array and 20 / a semiconductor laser chip and 24 ] V fluting Si substrates.

[0015] First, the 1st example of this invention is explained using drawing 1 - drawing 2. As shown in drawing 2 (a), a quartz substrate is used as a transparence substrate 1, many optical semiconductor chips 2 are mounted on this quartz substrate with a wafer condition, and, subsequently hermetic sealing of many optical semiconductor chips is carried out with the cap of an one wafer condition.

[0016] a process ---like -- the quartz substrate 1 top -- the lift-off method -- using -- titanium/gold (Ti/Au) the electrode pattern 3 is formed, then a plasma-CVD method is used -- the insulating airtight ring 5 which consists of Si<sub>3</sub>N<sub>4</sub> film is formed.

[0017] Next, flip chip bonding of the optical semiconductor chip which consists of a flip chip PIN diode with a monolithic lens is carried out two-dimensional one by one on the quartz substrate 1. In drawing 1, this optical semiconductor device has the activity section electrode pattern 7 also at the activity section 6 of optical semiconductor chip 2 front face, as shown in a sectional view, and it has one lens 9 which processed the substrate on four solder bumps and cores for soldering the optical semiconductor chip 2 to the transparence substrate 1 at the rear face of a chip 2 in the shape of the spherical surface.

[0018] Next, it pulls out with the activity section electrode pattern 7, and an electrode is connected with a golden wire. It goes into a closure process after this. A front face uses the silicon (Si) plate of a field (100) for the ingredient of a cap. This Si plate is etched in the water solution of caustic potash (KOH), and the ring-like heights 12 are formed in the location corresponding to the insulating airtight ring 5 of the transparence quartz substrate 1.

[0019] And in the shape of a ring, patterning of the cap solder bump 11 of tin (Sn) is vapor-deposited and carried out to the front face of heights 12, and she is formed in it. The cap solder bump 11 is pasted up on the good metal coat (for example, Au) 4 of solder wettability in piles, it heats at 200 degrees C, and a hermetic seal is carried out.

[0020] Next, only cap 10 is first cut on the outside of the insulating airtight ring 5 using a dicing saw, and the quartz substrate 1 is cut every optical semiconductor chip 2 after that. And the optical receiving set with which the hermetic seal of the optical semiconductor chip 2 which attaches an optical fiber 14 and consists of a photodiode as shown in

drawing 1 (b) was carried out is done.

[0021] In addition, since the relative-position precision of the optical semiconductor device 2 within the transparence substrate 1 is good, when what arranged the optical fiber 14 in the same pitch as the optical semiconductor device 2 is used, the thing which bundle up the photodiode arranged two-dimensional and the optical fiber 14 arranged two-dimensional per wafer, and can do it and for which optical coupling can be carried out cannot be overemphasized.

[0022] Next, drawing 3 explains the 2nd example. This invention uses the photodiode array 20 and sticks the optical fiber array 19 which carried out slanting polish of the tip on the transparence substrate 1.

[0023] In addition, after the lamination of the optical fiber array 19 divided the transparence substrate 1 into the chip substrate 13, it was performed. Other parts are the same as that of the 1st example. Drawing 3 (b) shows the sectional view cut in A-A' Rhine of drawing 3 (a).

[0024] Next, the 3rd example is an example which carried out the laminating of the glass substrate 21 which has required thickness, and used it in order to adjust the transparence substrate 1 and focal distance which used the ion-exchange method for the glass plate, and formed the lens 9, as shown in drawing 4. In addition, although omitted in drawing 4, it cannot be overemphasized that eye a hermetic seal is performed using the cap 10 the insulating airtight ring 5 and for hermetic seals like the 1st example.

[0025] Next, the 4th example is shown in drawing 5. It is optical fiber equipment 16a to the V groove of the substrate which stuck SiO<sub>2</sub> film (1a) for components equivalent to the components which combined the transparence substrate 1 and the optical fiber equipment 16 of said example in this example on the front face of the V fluting Si substrate 24. It replaces. In addition, although omitted in drawing 5, it cannot be overemphasized that eye a hermetic seal is performed using the cap 10 the insulating airtight ring 5 and for hermetic seals like the 1st example.

[0026] Next, drawing 6 shows the example which carries out the hermetic seal of the semiconductor laser using this invention. First, vacuum deposition of Ti and the Au is carried out to the front face of the transparence substrate 1 which formed the lens 9 in the glass plate by the ion-exchange method, bonding of the semiconductor laser chip 23 is carried out to it, the electrode pattern 3 for wiring further is formed in it, and the insulating airtight ring 5 and a coat 4 are formed in it after that.

[0027] Next, the three-layer spin coat of the polyimide film with which refractive indexes differ is carried out, and the optical waveguide 22 with a slanting mirror is formed using photolithography and dry etching. Next, bonding of the semiconductor laser chip 23 is carried out, and a hermetic seal is carried out with cap 10.

[0028] Since electric junction can be performed only by bonding in the case of the semiconductor laser chip 23, it is not necessary to perform wirebonding like an old example.

[0029] [Effect of the Invention] In this invention, since a wafer-like cap is too used for a hermetic seal as it is after mounting many optical semiconductor chips in a wafer-like transparence substrate first, the package closure is performed simply and mass production method of it is attained. Moreover, cap cost is reduced, in order to carry out Si wafer use and to perform projection formation under a cap on a cap per wafer too by etching. Consequently, the cost of an optical semiconductor device is reduced remarkably.

[0030] Moreover, effectiveness that optical semiconductor device declining becomes a thin shape like examples 2-4 since an optical fiber is set to a substrate and parallel, drawing 5 Since the reflective location of light is fixed by the approach, if an electrode pattern is formed in a desired location, optical coupling will be performed by no adjusting only by carrying out bonding of the chip 2. Moreover, since waveguide and an electrode pattern are formed with lithography by the approach of drawing 6, the location precision of a lens, waveguide, and an electrode pattern becomes high, and there is effectiveness -- optical coupling is performed by no adjusting.

## TECHNICAL FIELD

---

[Industrial Application] This invention relates to the hermetic seal into the manufacture approach of the luminescence equipment for optical communication which uses an optical semiconductor chip, and light-receiving equipment, especially the optical semiconductor device of an optical semiconductor chip.

## PRIOR ART

---

[Description of the Prior Art] Drawing 7 is the explanatory view of the conventional example. drawing -- setting -- 2 -- an optical semiconductor chip and 3 -- an electrode pattern and 6 -- the activity section and 7 -- an activity section electrode pattern and 8 -- a solder bump and 9 -- a lens and 10 -- a cap and 14 -- an optical fiber and 15 -- for a wire and 25, as for lead wire and 27, a block and 26 are [ light and 17 / a drawer electrode and 18 / an insulating material and 28 ] apertures.

[0003] Conventionally, as shown in drawing 7, after carrying out bonding of the optical semiconductor chip 2 to the block 25 to which lead wire 26 and electrode pattern 3 grade were attached, the transparent cap 10 with aperture 28 which penetrates the light 15 from an optical fiber 14 was welded to the block 25, and the hermetic seal was performed.

[0004]

## TECHNICAL PROBLEM

---

[Problem(s) to be Solved by the Invention] However, it is necessary to stick the chip-like aperture 28 on cap 10, and the process of shaping of an aperture 28, metallizing, and lamination is needed by such approach in that case. Therefore, the one-piece \*\*\*\*\* sake took time and effort every optical semiconductor chip 2 in these processes, and there was a problem that productivity was bad and the yield also fell.

[0005] Moreover, in order to make enlarging reinforcement of an aperture 28, and the coefficient of thermal expansion of an aperture 28 in agreement with cap 10, expensive ingredients, such as sapphire, were used for the ingredient of an aperture 27, and it was expensive also on the cap 10 and ingredients, such as covar with bad workability, were used for it.

[0006] Therefore, the problem that the cost of ingredient components became large was produced. Furthermore, by the conventional approach, since both the bonding of the

optical semiconductor chip 2 and every one hermetic seal of cap 10 were performed, the limitation was in mass-production nature.

[0007] This invention was offered in view of such a trouble, bundles up the hermetic seal of many optical semiconductor chips, performs it to coincidence, and aims at offering the manufacture approach of the optical semiconductor device which shortens a process.

## MEANS

---

[Means for Solving the Problem] Drawing 1 is the principle explanatory view of this invention, and drawing 2 is the explanatory view of the 1st example of this invention. drawing -- setting -- 1 -- a transparence substrate and 2 -- an optical semiconductor chip and 3 -- an electrode pattern and 4 -- a coat and 5 -- an insulating airtight ring and 6 -- the activity section and 7 -- an activity section electrode pattern and 8 -- a solder bump and 9 -- a lens and 10 -- a cap and 11 -- a cap solder bump and 12 -- for an optical fiber and 15, as for optical fiber equipment and 17, light and 16 are [ heights and 13 / a chip substrate and 14 / a drawer electrode and 18 ] wires.

[0009] In order to solve the above-mentioned trouble, after carrying a majority of two or more optical semiconductor chips 2 in the one wafer-like transparence substrate 1 two-dimensional by the approach of this invention, soldering the cap which consists of one substrate too by the approach of this invention and performing the package coincidence hermetic seal of an optical semiconductor chip, a cap and a transparence substrate are cut and an optical semiconductor device is obtained.

[0010] Namely, two or more electrode patterns 3 which have solder wettability on the transparence substrate 1 as the purpose of this invention is shown in drawing 1 (a), The process which forms the insulating airtight ring 5 on which the coat 4 which has solder wettability in the periphery of this electrode pattern 3 was put, The process which positions and solders this solder bump 8 of this optical semiconductor chip 2 that has two or more solder bumps 8 and the convex lens 9 at the rear face to this electrode pattern 2, As it is indicated in drawing 1 (b) as the process which solders this cap solder bump 11 of cap 10 that has the cap solder bump 11 to an inferior surface of tongue, and carries out the hermetic seal of this optical semiconductor chip 2 to this insulating airtight ring 5 By including the process which separates this cap 10 this each optical semiconductor chip 2 of every on the outside of this insulating airtight ring 5, then separates this transparence substrate 1 to the chip substrate 13 containing this each optical semiconductor chip 2 Moreover, as shown in drawing 2 (a), as shown in said transparence substrate 1 which arranged and was soldered on said transparence substrate 1 two-dimensional at drawing 1 (a), said two or more optical semiconductor chips 2 By carrying out alignment of the cap 10 which has said cap solder bump 11 formed in the inferior surface of tongue two-dimensional corresponding to said insulating ring 5, soldering it, and carrying out the hermetic seal of these two or more optical semiconductor chips 2 collectively Furthermore, as shown in the example of drawing 3 - drawing 6 , it is attained by pasting up the optical fiber equipment 16 which has a light reflex means to bend the optical axis of this optical fiber 14 on said transparence substrate 1 so that incidence of the light 15 by which outgoing radiation was carried out from the optical fiber 14 may be carried out to the lens 9 of said optical semiconductor chip 2.



## OPERATION

---

[Function] Since according to the means of this invention the transparence substrate with which many optical semiconductor chips were arranged two-dimensional, and much caps can use the cap arranged by two dimensions and can carry out a package hermetic seal now per wafer, productive efficiency goes up compared with the former, and the yield also improves.

[0012] Moreover, since batch processing also of metallizing processing of an aperture ingredient, bonding, and the wiring can be carried out now per wafer, it is suitable for mass production method. And since the surface mount gestalt is taken, it is effective in it becoming easy to automate bonding using the mounting equipment for mounting components to up to the conventional printed circuit board. As a result, low cost-ization is realizable.

## EXAMPLE

---

[Example] Drawing 1 is the explanatory view of some examples of this invention, and shows the principle explanatory view of this invention, drawing 2 - drawing 6 except for the perspective view of drawing 2 in a type section Fig.

[0014] In drawing 1 an optical semiconductor chip and 3 for a transparence substrate and 2 An electrode pattern, In 4, a coat and 5 the activity section and 7 for an insulating airtight ring and 6 An activity section electrode pattern, In 8, a solder bump and 9 a cap and 11 for a lens and 10 A cap solder bump, For a chip substrate and 14, an optical fiber and 15 are [ 12 / heights and 13 ] light, and 16 and 16a. Optical fiber equipment, 17 -- a drawer electrode and 18 -- for a photodiode array and 21, as for optical waveguide and 23, a glass substrate and 22 are [ a wire and 19 / an optical fiber array and 20 / a semiconductor laser chip and 24 ] V fluting Si substrates.

[0015] First, the 1st example of this invention is explained using drawing 1 - drawing 2 . As shown in drawing 2 (a), a quartz substrate is used as a transparence substrate 1, many optical semiconductor chips 2 are mounted on this quartz substrate with a wafer condition, and, subsequently hermetic sealing of many optical semiconductor chips is carried out with the cap of an one wafer condition.

[0016] a process ---like -- the quartz substrate 1 top -- the lift-off method -- using -- titanium/gold (Ti/Au) the electrode pattern 3 is formed, then a plasma-CVD method is used -- the insulating airtight ring 5 which consists of Si<sub>3</sub>N<sub>4</sub> film is formed.

[0017] Next, flip chip bonding of the optical semiconductor chip which consists of a flip chip PIN diode with a monolithic lens is carried out two-dimensional one by one on the quartz substrate 1. In drawing 1 ; this optical semiconductor device has the activity section electrode pattern 7 also at the activity section 6 of optical semiconductor chip 2 front face, as shown in a sectional view, and it has one lens 9 which processed the substrate on four solder bumps and cores for soldering the optical semiconductor chip 2 to the transparence substrate 1 at the rear face of a chip 2 in the shape of the spherical surface.

[0018] Next, it pulls out with the activity section electrode pattern 7, and an electrode is connected with a golden wire. It goes into a closure process after this. A front face uses

the silicon (Si) plate of a field (100) for the ingredient of a cap. This Si plate is etched in the water solution of caustic potash (KOH), and the ring-like heights 12 are formed in the location corresponding to the insulating airtight ring 5 of the transparence quartz substrate 1.

[0019] And in the shape of a ring, patterning of the cap solder bump 11 of tin (Sn) is vapor-deposited and carried out to the front face of heights 12, and she is formed in it. The cap solder bump 11 is pasted up on the good metal coat (for example, Au) 4 of solder wettability in piles, it heats at 200 degrees C, and a hermetic seal is carried out.

[0020] Next, only cap 10 is first cut on the outside of the insulating airtight ring 5 using a dicing saw, and the quartz substrate 1 is cut every optical semiconductor chip 2 after that. And the optical receiving set with which the hermetic seal of the optical semiconductor chip 2 which attaches an optical fiber 14 and consists of a photodiode as shown in drawing 1 (b) was carried out is done.

[0021] In addition, since the relative-position precision of the optical semiconductor device 2 within the transparence substrate 1 is good, when what arranged the optical fiber 14 in the same pitch as the optical semiconductor device 2 is used, the thing which bundle up the photodiode arranged two-dimensional and the optical fiber 14 arranged two-dimensional per wafer, and can do it and for which optical coupling can be carried out cannot be overemphasized.

[0022] Next, drawing 3 explains the 2nd example. This invention uses the photodiode array 20 and sticks the optical fiber array 19 which carried out slanting polish of the tip on the transparence substrate 1.

[0023] In addition, after the lamination of the optical fiber array 19 divided the transparence substrate 1 into the chip substrate 13, it was performed. Other parts are the same as that of the 1st example. Drawing 3 (b) shows the sectional view cut in A-A' Rhine of drawing 3 (a).

[0024] Next, the 3rd example is an example which carried out the laminating of the glass substrate 21 which has required thickness, and used it in order to adjust the transparence substrate 1 and focal distance which used the ion-exchange method for the glass plate, and formed the lens 9, as shown in drawing 4. In addition, although omitted in drawing 4, it cannot be overemphasized that eye a hermetic seal is performed using the cap 10 the insulating airtight ring 5 and for hermetic seals like the 1st example.

[0025] Next, the 4th example is shown in drawing 5. It is optical fiber equipment 16a to the V groove of the substrate which stuck SiO<sub>2</sub> film (1a) for components equivalent to the components which combined the transparence substrate 1 and the optical fiber equipment 16 of said example in this example on the front face of the V fluting Si substrate 24. It replaces. In addition, although omitted in drawing 5, it cannot be overemphasized that eye a hermetic seal is performed using the cap 10 the insulating airtight ring 5 and for hermetic seals like the 1st example.

[0026] Next, drawing 6 shows the example which carries out the hermetic seal of the semiconductor laser using this invention. First, vacuum deposition of Ti and the Au is carried out to the front face of the transparence substrate 1 which formed the lens 9 in the glass plate by the ion-exchange method, bonding of the semiconductor laser chip 23 is carried out to it, the electrode pattern 3 for wiring further is formed in it, and the insulating airtight ring 5 and a coat 4 are formed in it after that.

[0027] Next, the three-layer spin coat of the polyimide film with which refractive indexes

differ is carried out, and the optical waveguide 22 with a slanting mirror is formed using photolithography and dry etching. Next, bonding of the semiconductor laser chip 23 is carried out, and a hermetic seal is carried out with cap 10.

[0028] Since electric junction can be performed only by bonding in the case of the semiconductor laser chip 23, it is not necessary to perform wirebonding like an old example.

## EFFECT OF THE INVENTION

[Effect of the Invention] In this invention, since a wafer-like cap is too used for a hermetic seal as it is after mounting many optical semiconductor chips in a wafer-like transparence substrate first, the package closure is performed simply and mass production method of it is attained. Moreover, cap cost is reduced, in order to carry out Si wafer use and to perform projection formation under a cap on a cap per wafer too by etching. Consequently, the cost of an optical semiconductor device is reduced remarkably.

[0030] Moreover, effectiveness that optical semiconductor device declining becomes a thin shape like examples 2-4 since an optical fiber is set to a substrate and parallel, drawing 5 Since the reflective location of light is fixed by the approach, if an electrode pattern is formed in a desired location, optical coupling will be performed by no adjusting only by carrying out bonding of the chip 2. Moreover, since waveguide and an electrode pattern are formed with lithography by the approach of drawing 6, the location precision of a lens, waveguide, and an electrode pattern becomes high, and there is effectiveness -- optical coupling is performed by no adjusting.

## DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] The principle explanatory view of this invention

[Drawing 2] The explanatory view of the 1st example of this invention

[Drawing 3] The explanatory view of the 2nd example of this invention

[Drawing 4] The explanatory view of the 3rd example of this invention

[Drawing 5] The explanatory view of the 4th example of this invention

[Drawing 6] The explanatory view of the 5th example of this invention

[Drawing 7] The explanatory view of the conventional example

[Description of Notations]

1 Transparence Substrate

1a SiO<sub>2</sub> film

2 Optical Semiconductor Chip

3 Electrode Pattern

4 Coat

5 Insulating Airtight Ring

6 Activity Section

7 Activity Section Electrode Pattern

8 Solder Bump

9 Lens

10 Cap  
11 Cap Solder Bump  
12 Heights  
13 Chip Substrate  
14 Optical Fiber  
15 Light  
16 16a Optical fiber equipment  
17 Drawer Electrode  
18 Wire  
19 Optical Fiber Array  
20 Photodiode Array  
21 Glass Substrate  
22 Optical Waveguide  
23 Semiconductor Laser Chip  
24 V Fluting Si Substrate

## CLAIMS

---

### [Claim(s)]

[Claim 1] transparence substrate (1) Two or more electrode patterns (3) which have solder wettability upwards This electrode pattern (3) Coat which has solder wettability in a periphery (4) Put insulating airtight ring (5) The process to form, Solder bump of plurality [ rear face ] (8) Convex lens (9) This optical semiconductor chip that it has (2) This solder bump (8) This electrode pattern (2) The process positioned and soldered, This insulating airtight ring (5) This cap solder bump (11) of a cap (10) that has a cap solder bump (11) is soldered to an inferior surface of tongue, and it is this optical semiconductor chip (2). The process which carries out a hermetic seal, this cap (12) -- this insulating airtight ring (5) an outside -- this each optical semiconductor chip (2) It separates. every - - Then, this transparence substrate (1) This each optical semiconductor chip (2) The manufacture approach of the optical semiconductor device characterized by including the process separated to the included chip substrate (13).

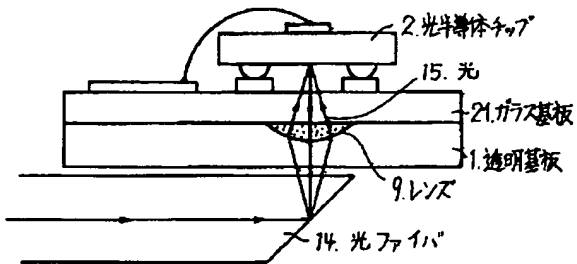
[Claim 2] said two or more optical semiconductor chips (2) two-dimensional -- said transparence substrate (1) Said transparence substrate (1) which arranged upwards and was soldered to it It is said insulating ring (5) to an inferior surface of tongue. Carry out alignment of the cap (10) which has said cap solder bump (11) who corresponded and was formed two-dimensional, and it is soldered. These two or more optical semiconductor chips (2) The manufacture approach of the optical semiconductor device according to claim 1 characterized by carrying out a hermetic seal collectively.

[Claim 3] About the light (15) by which outgoing radiation was carried out from the optical fiber (14), it is said optical semiconductor chip (2). Lens (9) It is said transparence substrate (1) about the optical fiber equipment (16) which has a light reflex means to bend the optical axis of this optical fiber (14) so that incidence may be carried out. The manufacture approach of claim 1 characterized by pasting up, or an optical semiconductor device according to claim 2.

DRAWINGS

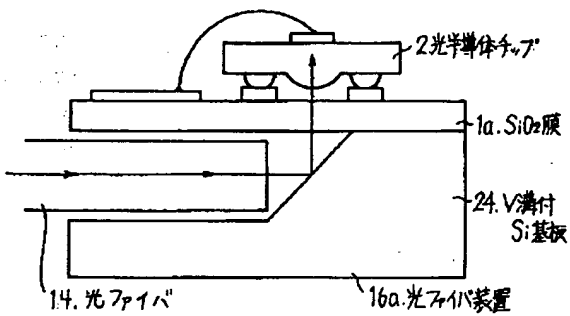
[Drawing 4]

本発明の第3の実施例の説明図



[Drawing 5]

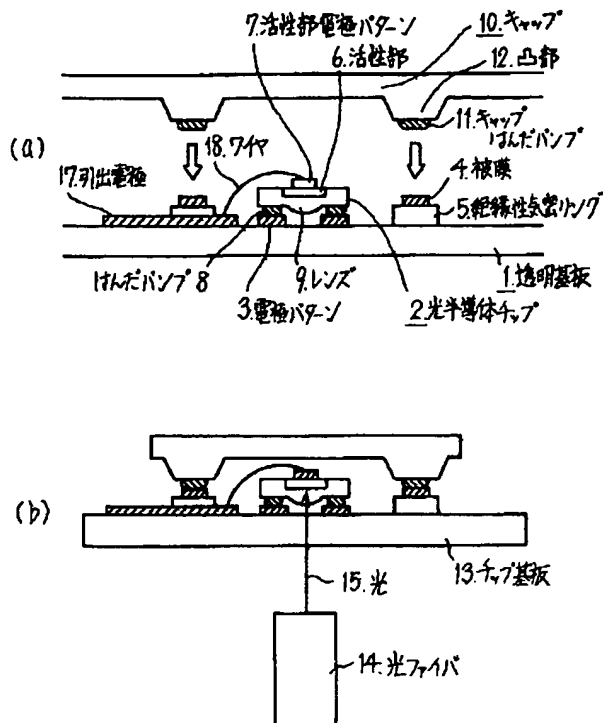
本発明の第4の実施例の説明図



[Drawing 1]

**BEST AVAILABLE COPY**

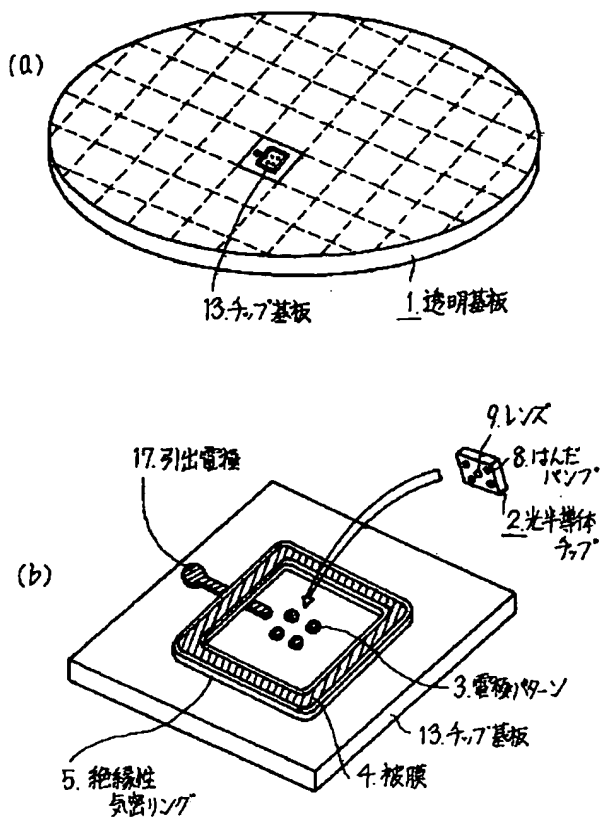
### 本発明の原理説明図



[Drawing 2]

**BEST AVAILABLE COPY**

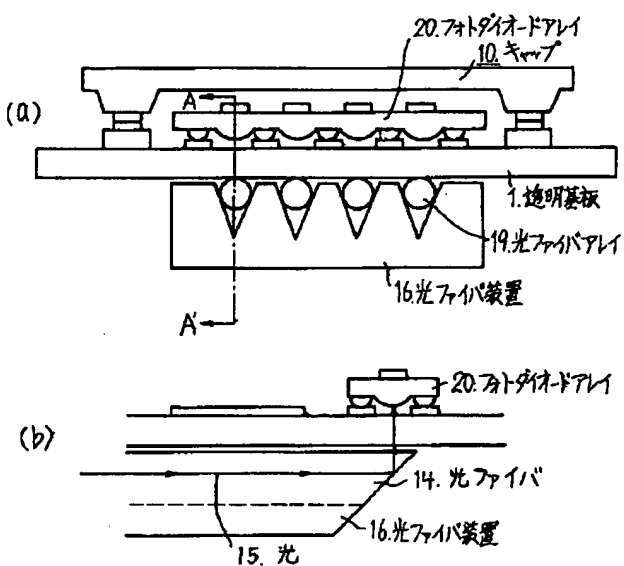
本発明の第1の実施例の説明図



BEST AVAILABLE COPY

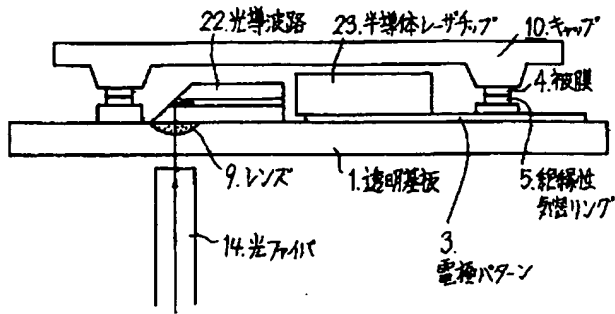
[Drawing 3]

本発明の第2の実施例の説明図



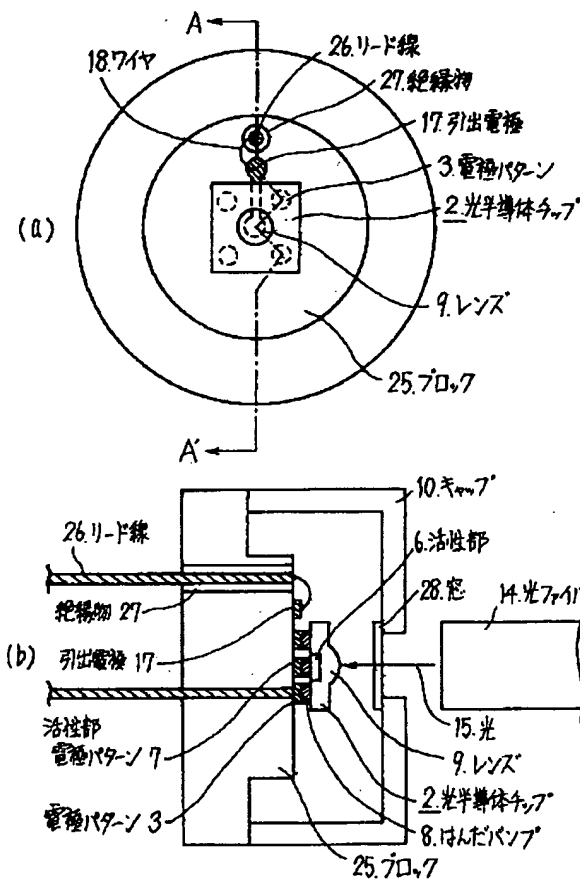
[Drawing 6]

本発明の第5の実施例の説明図



[Drawing 7]

従来例の説明図





**Translation of the relevant portions of Reference 1**  
**Japanese Patent Unexamined Publication No. 60-153184**

**Please see the English abstract of Reference 1**

**The content of the English abstract of Reference 1 substantially correspond to the relevant portions of Reference 1, line 18 in the top left column to line 1 in the bottom right column in page 3 thereof.**

**Appendix;**

**Reference number 48 indicates an optical fiber.**

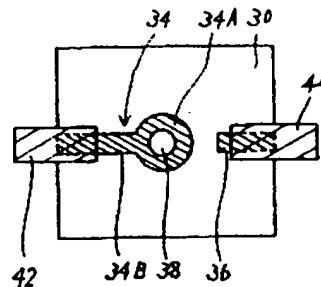
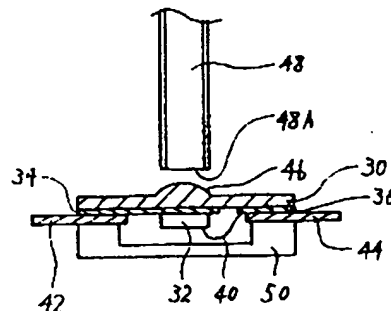
PUBLICATION NUMBER : 60153184  
PUBLICATION DATE : 12-08-85  
  
APPLICATION DATE : 21-01-84  
APPLICATION NUMBER : 59007940

APPLICANT : SUMITOMO ELECTRIC IND LTD;

INVENTOR : KURODA MASATAKA;

INT.CL. : H01L 31/02 G02B 6/42

TITLE : LIGHT RECEIVING ELEMENT



ABSTRACT : PURPOSE: To obtain the titled element having a small interterminal static capacitance and unnecessitating high accuracies in the positioning of a light receiving element chip to the lens center by a method wherein a substrate is thinned and a condenser lens is made integral with the substrate, and an insulator package is used for the light receiving element chip.

CONSTITUTION: The substrate 30 of the illustrated light receiving element is made of insulating glass which is optically transparent in a light receiving wavelength band and chemically stable. A photoelement chip 32 is fixed to the lower surface of this substrate 30, and bonding pads 34 and 36 are formed. The pad 34 has a circular part 34A, and a photo receiving window 38 is formed at the center of this part 34A. The electrode around the photo receiving window of the chip 32 is diebonded to the circular part 34A of the pad 34 so that the photo receiving plane of the chip 32 may be coincident with the window 38. On the other hand, the electrode on the opposite side of the photo receiving plane of the chip 32 is connected to the pad 36 with a wire 40, and outer leads 42 and 44 are connected to the pads 34 and 36, respectively. The condenser lens 46 is integrally formed to the upper surface of the substrate 30 in agreement with the window 38. Further, the chip 32 is encircled and the peripheral edge of a cap 50 is hermetically sealed to the lower surface of the substrate, thus completing the titled element.

COPYRIGHT: (C)1985,JPO&Japio

BEST AVAILABLE COPY

⑩ 日本国特許庁(JP)

⑪ 特許出願公開

⑫ 公開特許公報(A) 昭60-153184

⑬ Int.Cl.<sup>4</sup>

識別記号

庁内整理番号

⑭ 公開 昭和60年(1985)8月12日

H 01 L 31/02

7216-5F

G 02 B 6/42

7529-2H

審査請求 未請求 発明の数 1 (全5頁)

⑮ 発明の名称 受光素子

⑯ 特 願 昭59-7940

⑰ 出 願 昭59(1984)1月21日

⑱ 発 明 者 黒 田 正 孝 大阪市此花区島屋1丁目1番3号 住友電気工業株式会社  
大阪製作所内

⑲ 出 願 人 住友電気工業株式会社 大阪市東区北浜5丁目15番地

⑳ 代 理 人 弁理士 新居 正彦

明細書

1. 発明の名称 受光素子

2. 特許請求の範囲

(1) 受光波長帯域で透明な絶縁性の基材と、該基材の一方の面に受光面が位置するように該基材に対して固定された受光素子チップと、該受光素子チップの各電極部に接続された外部リードと、前記受光素子チップを囲むように前記基材に封止された絶縁性の封止体と、前記受光素子チップの前記受光面に一致するように前記基材の前記一方の面と対向する面に一体的に設けられた集光レンズとを具備することを特徴とする受光素子。

(2) 前記受光素子チップは、受光面を囲むように一方の電極が形成されており、該受光面と反対側の面に他方の電極が形成されており、前記受光素子チップの前記受光面側電極は、前記基材の一方の面に受光面を残すように形成されたメタライズ

ボンディングパッドにボンディングされていることを特徴とする特許請求の範囲第1項記載の受光素子。

(3) 前記受光素子チップは、受光面を囲むように一方の電極が形成されており、該受光面と反対側の面に他方の電極が形成されており、前記受光素子チップの前記受光面側電極は、前記基材の一方の面に形成された受光波長領域において実質的に透明な導電材料層にボンディングされていることを特徴とする特許請求の範囲第1項記載の受光素子。

(4) 前記封止体は、セラミック又はプラスチックで作られてキャップ状をしており、そのカップの周縁部が前記基材の前記一方の面に気密固定されていることを特徴とする特許請求の範囲第1から第3項までのいずれかに記載の受光素子。

(5) 前記封止体は、前記基材の前記一方の面全体

に密着してプラスチック封止しているプラスチックモールドであることを特徴とする特許請求の範囲第1から第3項までのいずれかに記載の受光素子。

(6) 前記基材は、ガラス又はサファイヤで作られていることを特徴とする特許請求の範囲第1項から第5項までのいずれかに記載の受光素子。

(7) 前記集光レンズは、前記基材と同一材料で作られていることを特徴とする特許請求の範囲第1項から第6項までのいずれかに記載の受光素子。

### 3. 発明の詳細な説明

#### 産業上の利用分野

本発明は、受光素子に関するものであり、更に具体的には、受光素子のパッケージング構造の改良に関するものである。

プ10の受光面に入射する。

上記した構造において、受光素子チップ10が金属パッケージ12にダイボンディングされているために、受光素子チップと金属パッケージとの電位差により静電容量が生じ、端子間静電容量が大きく、高速動作に適していない。

また、レンズ窓20と受光素子チップ10の受光面との距離が1mm程度離れているために、レンズ窓20を通して入射した光が受光素子チップ10の受光面に十分入射されるように、レンズ窓20と受光素子チップ10の受光面とを正確に軸合わせする必要がある。この軸合わせの問題を考える場合、レンズ窓20はキャップ22の所定の場所に設けられているので、パッケージング終了後金属パッケージ12に対して所定の位置にくる。それ故、受光素子チップ10を金属パッケージ12の所定位置に正確にダイボンディングする必要がある。しかし、正確にダイボンディングすることは非常に難しく且つ手間がかかるために、受光素子の価格が高くなる問題がある。

### 特開昭60-153184 (2)

#### 従来技術

従来の受光素子のパッケージング構造の典型例の一つを示すと、第1図の如きである。第1図において、受光素子チップ10は、受光面を囲むように一方の電極が形成されており、受光面と反対側の面には他方の電極が形成される。そして、その受光素子チップ10は、受光面を上にして、他方電極が金属パッケージ12にボンディングされている。その金属パッケージ12からは、金属パッケージ12自体に接続したリード14が垂下しており、更に、金属パッケージ12に対して絶縁されたもう1つのリード16が貫通して垂下している。そのリード16の上端は、ワイヤ18を介して受光素子チップ10の一方の電極に接続されている。

そのように受光素子チップ10が固定されているパッケージ12には、レンズ窓20が形成されている。キャップ22が装着され、受光素子チップ10が金属パッケージ12とキャップ22との間に封止されている。従って、例えば、光ファイバ24の端面から入射される光は、レンズ窓20を通して受光素子チッ

#### 発明の目的

そこで、本発明は、端子間静電容量が小さく且つ受光素子チップとレンズ中心位置との位置合わせに高精度を要しないパッケージング構造の受光素子を提供せんとするものである。

#### 発明の構成

すなわち、本発明によるならば、受光波長帯域で透明な絶縁性の基材と、該基材の一方の面に受光面が位置するように該基材に対して固定された受光素子チップと、該受光素子チップの各電極部に接続された外部リードと、前記受光素子チップを囲むように前記基材に封止された絶縁性の封止体と、前記受光素子チップの前記受光面に一致するように前記基材の前記一方の面と対向する面に一体的に設けられた集光レンズとを具備することを特徴とする受光素子が提供される。

以上の如き構成にするならば、金属パッケージをなくすることができるので、受光素子チップとそれがダイボンディングされた金属パッケージとの間の静

電容量に相当する分だけ受光素子の端子間静電容量が小さくなり、全体の静電容量を著しく小さくできる。

更に、集光レンズと受光素子チップが両側に設けられる基材を薄くすることにより、集光レンズと受光素子チップの受光面との距離が大幅に短縮されるので、光案内の光放射端面と受光素子チップの受光面とを大幅に近づけることができるために、受光素子チップと集光レンズとの位置合わせ即ち受光素子チップの基材に対するダイボンディングに、従来の受光素子におけるほどボンディングの緻密さが要求されない。

#### 実施例

以下添付図面を参照して本発明による受光素子の実施例を説明する。

第2図は、本発明による受光素子の概略断面図である。

図示の受光素子は、板状の基材30を有しており、その基材30は、受光波長帯域において光学的に透

#### 特開昭60-153184(3)

明で且つ化学的に安定で機械的に十分な強度を有する絶縁材料、例えば、ガラスやサファイヤなどから作られている。

そのような基材30の一方の面、第2図においては下面は、第1図の受光素子チップ10と同様な受光素子チップ32が固定される側である。その基材30の下面は、第3図に示す如く、メタライズ処理により2つボンディングパッド34および36が形成されている。一方のボンディングパッド34は、基材30の中央に位置する円形部34Aを有しており、それから帯状部34Bが基材30の一边の縁まで延びている。そして、円形部34Aの中央には、受光窓38が形成されている。

他方のボンディングパッド36は、一方のボンディングパッド34の帯状部34Bが終端している基材30の辺と向い合う一边から、一方のボンディングパッド34の円形部34Aに向かって延びている。しかし、ボンディングパッド36は、円形部34Aから十分離れた所、具体的には受光素子チップ32をボンディングした時に受光素子チップがボンディン

グパッド36に接しない様十分大きい距離離れた所で終端している。

そのようなボンディングパッド34の円形部34Aの受光窓38に受光素子チップ32の受光面が一致するように、受光素子チップ32の受光面の周りの電極がボンディングパッド34の円形部34Aにダイボンディングされる。一方、受光素子チップ32の受光面と反対側の電極は、ワイヤ40によりボンディングパッド36に接続されている。そして、ボンディングパッド34と36には、外部リード42および44がそれぞれ接続されている。

基材30の反対側の面即ち上面には、受光窓38と一致させて集光レンズ46が一体的に形成されている。この集光レンズ46は、例えば光ファイバ48のような光案内の出射端48Aからの入射光を、受光素子チップ32の受光面に適当な大きさに集光させるように働く。

更に、受光素子チップ32を囲むように、キャップ50の周縁が基材30の下面に気密封止されている。このキャップ50は、例えばセラミックやプラスチック

等の絶縁材料で作られる。

以上の如く構成される受光素子において、基材30を例えば100～300 $\mu$ m程度の厚さにできる。従って、基材30の両側に設けられる集光レンズ46と受光素子チップ32との距離は、従来に比較して1/10から1/3に短縮されている。従って、光ファイバ48の出射端48Aと受光素子チップ32の受光面とをその分近接させてその間の光エネルギーの消散を少なくすることができるので、集光レンズ46と受光素子チップ32の受光面との軸合わせ即ち受光素子チップ32の基材30に対するダイボンディングの位置精度が従来例ほど要求されない。

更に、集光レンズ46が基材30と一体構造であるので、受光窓38と集光レンズ46とが予め高精度で位置合わせできる。それ故、受光窓38の周囲のボンディングパッドの円形部34Aに受光素子チップをボンディングするだけで、集光レンズ46に対して受光素子チップの受光面を軸合わせできる。

また、金属パッケージでなく絶縁体パッケージを使用しているので、静電容量が著しく小さくな

されている。

なお、上記実施例においては、受光素子チップが、基材30の一方の面に受光窓38を残すように形成されたメタライズボンディングパッド34にダイボンディングされている。しかし、基材30のその一方の面に、受光波長領域において実質的に透明な導電材料層を形成し、その導電性材料層に受光素子チップの受光面側電極をボンディングしてもよい。

また、上記実施例においては、セラミック又はプラスチックで作られたキャップ50の周縁部が基材30のその一方の面に気密固定されているが、その基材30の一方の面全体にプラスチックモールドを密着させてプラスチック封止してもよい。

更に、集光レンズ46は、基材30と同一材料で作られていることが好ましいが、異なる材料で作られてもよい。後者の場合、集光レンズ46と基材30との界面が反射面を形成するが、その反射率が低ければ問題はない。

示す概略断面図、第2図は本発明による受光素子のパッケージング構造を示す概略断面図、そして、第3図は第2図の受光素子の基材の下面のボンディングパッドパターンを示す図である。

(主な参照番号)

- 10・・・受光素子チップ、
- 12・・・金属パッケージ、
- 14、16・・・リード、 18・・・ワイヤ、
- 20・・・レンズ窓、 22・・・キャップ、
- 24・・・光ファイバ、 30・・・基材、
- 32・・・受光素子チップ、
- 34、36・・・ボンディングパッド、
- 38・・・受光窓、 40・・・ワイヤ、
- 42、44・・・リード、 46・・・集光レンズ、
- 48・・・光ファイバ、 50・・・キャップ

特許出願人 住友電気工業株式会社  
代理人 弁理士 新居正彦

特開昭60-153184(4)

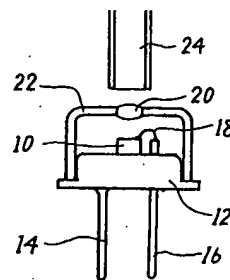
#### 発明の効果

以上の如く、本発明によるならば、金属パッケージをなくすることができるので、受光素子チップとそれがダイボンディングされた従来の金属パッケージとの間の静電容量に相当する分だけ受光素子の端子間静電容量が小さくなり全体の静電容量が著しく小さくされている。従って、高速動作が可能となる。

更に、集光レンズと受光素子チップが両側に設けられる基材を薄くすることにより、集光レンズと受光素子チップ受光面との距離が大幅に短縮されるので、光案内の出射端と受光素子チップとの距離を小さくするとにより光射端よりの光をそのエネルギー損失少なく受光素子の受光面へ入射させることができるため、受光素子チップの基材に対するダイボンディングの精度に、従来の受光素子におけるほどの厳密さが要求されない。

#### 4. 図面の簡単な説明

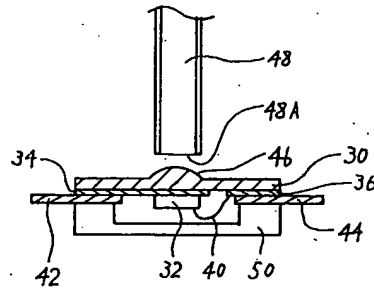
第1図は従来の受光素子パッケージング構造を



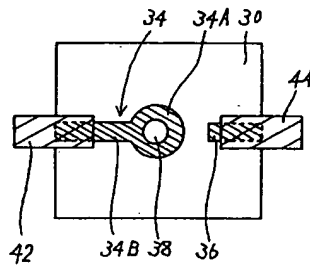
第1図

BEST AVAILABLE COPY

特開昭60-153184(5)



第2図



第3図

**This Page is Inserted by IFW Indexing and Scanning  
Operations and is not part of the Official Record**

**BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ **BLACK BORDERS**
- ☐ **IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- ☐ **FADED TEXT OR DRAWING**
- ☐ **BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- ☐ **SKEWED/SLANTED IMAGES**
- ☐ **COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- ☐ **GRAY SCALE DOCUMENTS**
- ☒ **LINES OR MARKS ON ORIGINAL DOCUMENT**
- ☐ **REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- ☐ **OTHER:** \_\_\_\_\_

**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.**